



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,406	08/22/2003	Tsung-Liang Lin	251316-1770	9248
24504 7590 04/21/2008 THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP 600 GALLERIA PARKWAY, S.E. STE 1500 ATLANTA, GA 30339-5994				
EXAMINER				
DEPPEL, BETSY LEE				
ART UNIT		PAPER NUMBER		
2611				
MAIL DATE		DELIVERY MODE		
04/21/2008		PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/646,406

**Applicant(s)**

LIN ET AL.

**Examiner**

BETSY L. DEPPE

**Art Unit**

2611

**Period for Reply** -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 March 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4, 6-12 and 14-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-12 and 14-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/S508)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments filed March 3, 2008 have been fully considered.
2. In response to applicant's argument on pages 8 and 9 that the examiner has combined an excessive number of references, reliance on a large number of references in a rejection does not, without more, weigh against the obviousness of the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991).
3. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

On page 8 of the remarks, the applicant further argues that "it is clear that the alleged motivation took the content of Applicant's disclosure as the reasoning for combining the references" regarding the Examiner's conclusion of obviousness. The Examiner traverses this assertion since, at the time the claimed invention was made, it

Art Unit: 2611

was known in the art that noise can be reduced by using separate circuit grounds for analog and digital circuits within an IC. (For example, see Sahota et al. (US Patent No. 6,615,027), column 2, lines 37-39) Furthermore, Joshi et al. (US Patent No. 5,650,754 cited in the Office Action mailed July 17, 2007), which was used in the rejection of the claims in the Office Action mailed December 5, 2007, recognizes the need to eliminate unwanted noise and interference. (See column 1, lines 38-40) Therefore, motivation for combining the references is not "gleaned only from the applicant's disclosure" (*emphasis added*) and the examiner's conclusion of obviousness is not based upon improper hindsight reasoning.

4. Applicant's arguments, see page 9, filed March 3, 2008, with respect to the rejection(s) of claim(s) 1 and 9 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the references in view of Antoniak (US Pub. No. 2003/0152140 A1).

### ***Claim Objections***

5. Claims 1, 9 and 12 are objected to because of the following informalities:

- a. in claim 1, line 25 and claim 9, line 22, a comma should be inserted after "synthesizer";
  - b. in claim 1, line 26 and claim 9, line 22, "controller" should be "controlled";
- and

- c. in claim 12, line 1, "lock" should be "clock".

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
7. Claims 1, 2, 4, 7-10, 12, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antoniak (US Pub. No. 2003/0152140 A1), Isley, Jr. et al. (US Patent No. 5,930,295 cited in the Office Action mailed November 24, 2006) in view of Robinson et al. (US Patent No. 5,943,290 cited in the Office Action mailed November 24, 2006), Joshi et al. (US Patent No. 5,650,754 cited in the Office Action mailed July 17, 2007), and Dent (US Patent No. 7,133,647 cited in the Office Action mailed July 17, 2007).
8. With regard to claims 1, 4, 9 and 12, Figure 1 of Isley, Jr. et al. discloses the claimed invention including a medium within which a communication signal propagates through (14), an analog circuit (e.g. any of the components that are part of 18), a digital circuit (20), an A/D interface circuit (28), a D/A interface circuit (34), a down-converter (26), an up-converter (32) and a synthesizer (24) coupled to a baseband processor (20). (See column 2, line 42- column 3, line 13 and column 4, lines 20-41) However, Isley, Jr. et al. does not disclose a switch for transmitting and receiving the communication signal in different time periods, the synthesizer comprised of a voltage controlled oscillator, a first ground reference, a second ground reference, and a joint clock source.

Since Antoniak discloses that a transceiver can operate as full-duplex (i.e. data transmission in both directions simultaneously) or half-duplex (i.e. data transmission in both directions but not at the same time) (see paragraph [0009]), i.e. the modes of operation are interchangeable, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the diplexer for full duplex operation in Isley, Jr. et al. with a switch for half-duplex operation (as taught by Antoniak) in order to enable the transmission or reception of more data at the same time via half-duplex mode. Whether the transceiver operates in full-duplex or half-duplex mode does not affect the operation of the components (e.g. the A/D or D/A circuit, up-converter or down-converter) within the transceiver.

Furthermore, Figure 1 of Antoniak discloses a synthesizer (52) comprised of a voltage controlled oscillator. It would have also been obvious to one of ordinary skill in the art at the time the invention was made to use a voltage controlled oscillator in the synthesizer of Isley, Jr. et al. in order to use a well-known and readily available component for generating frequency signals for the down-converter and up-converter, respectively.

Figure 1 of Robinson et al. discloses an integrated circuit with a joint clock source that provides signals to an analog circuit (12) and a digital circuit (14) wherein the analog circuit has a first ground reference (AGND), the digital circuit has a second ground reference (DGND) and a joint clock source (see XTAL in Figure 4) that supplies clock pulses to the analog circuit (including elements 42, 44 and Analog Portion in Figure 4) and the digital circuit (including elements 56, 58 and Digital Portion in Figure

4). (See column 1, lines 19-23; column 2, lines 1-26; column 3, lines 63-67; and column 4, line 65 - column 5, line 3) Since it is implicit that the transceiver/modem of Isley, Jr. et al. in view of Antoniak requires clocking signals, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Robinson et al. with Isley, Jr. et al. in view of Antoniak by implementing the transceiver of Isley, Jr. et al. in view of Antoniak as an integrated circuit with the separate ground references (as taught by Robinson et al.) in order to reduce the size of the transceiver while minimizing the noise between the digital and analog portions of the integrated transceiver circuit. Furthermore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a joint clock source to provide the clock signals to the various components in Isley, Jr. et al. (e.g. the A/D converter and D/A converter in analog circuit 18) in view of Antoniak in order to minimize the number of oscillators or clock sources needed for the circuit thereby further reducing the size of the transceiver.

However, Isley, Jr. et al. in view of Antoniak and Robinson et al. does not teach connecting the joint clock source directly to the first ground reference and not connecting the joint clock source directly to the second ground reference. Joshi et al. discloses connecting a VCO to an analog ground with separate grounding for other components. (See Figure 4 and column 7, line 60 - column 8, line 8) Since VCOs are crystal oscillators (see Dent, column 1, lines 12-13), it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the crystal

oscillator of Robinson et al. to the analog ground (as taught by Joshi et al.) in order to minimize noise.

9. With regard to claims 2 and 10, Isley, Jr. et al. in view of Antoniak, Robinson et al., Joshi et al. and Dent discloses the claimed invention including an antenna and propagating the signal through the air. (See Isley, Jr. et al., "14" in Figure 1)

10. With regard to claims 7 and 15 Isley, Jr. et al. in view of Antoniak, Robinson et al., Joshi et al. and Dent discloses the claimed invention including an analog-to-digital convertor. (See Isley, Jr. et al., "28" in Figure 1)

11. With regard to claims 8 and 16, Isley, Jr. et al. in view of Antoniak, Robinson et al., Joshi et al. and Dent discloses the claimed invention including a digital-to-analog convertor. (See Isley, Jr. et al., "34" in Figure 1)

12. Claims 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isley, Jr. et al in view Antoniak, Robinson et al., Joshi et al. and Dent as applied to claims 1 and 9, respectively, above, and further in view of Hoobler (US Patent No. 7,130,337 B2 cited in the Office Action mailed November 24, 2006). Isley, Jr. et al. in view of Antoniak, Robinson et al., Joshi et al. and Dent discloses the claimed invention except for propagating the communication signal through a wire.

Hoobler discloses that modems may be used in RF (i.e. over the air) systems or in power line systems (i.e. over a wire). (See column 3, lines 62-63) It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the invention disclosed by Isley, Jr. et al. in view of Antoniak, Robinson et al., Joshi et



al. and Dent in order to reduce noise of modems in wired communication systems.

Whether the modem is implemented in a RF or wired communication system does not affect the functionality or operability of the modem itself.

13. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isley, Jr. et al in view of Antoniak, Robinson et al., Joshi et al. and Dent, as applied to claims 1 and 9, respectively, above, and further in view of Sorrells et al. (US Pub. No. 2004/0013177 A1 cited in the Office Action mailed November 24, 2006). Isley, Jr. et al. in view of Antoniak, Robinson et al., Joshi et al. and Dent discloses the claimed invention except for a MAC unit.

Figure 3B of Sorrells et al. shows an integrated transceiver (322) interfacing with a MAC unit (112). Since the protocol or standard to the communication system does not affect the functionality or operation of the integrated transceiver circuit, it would have been obvious matter of design choice to one of ordinary skill in the art at the time the invention was made to implement the method or circuit disclosed by Isley, Jr. et al. in view of Antoniak, Robinson et al., Joshi et al. and Dent in a system that operates in accordance with such as IEEE 802.11 standards in order to optimize the performance of such a system by reducing noise caused by an integrated transceiver. Furthermore, in order for the integrated transceiver circuit to properly interface with controller of such a system, it is implicit that a MAC unit must be connected to the integrated transceiver circuit. (See Sorrells et al., paragraphs [0045]-[0046])

***Conclusion***

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to BETSY L. DEPPE whose telephone number is (571) 272-3054. The examiner can normally be reached on Monday, Wednesday and Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Betsy L. Deppe/  
Primary Examiner  
Art Unit 2611